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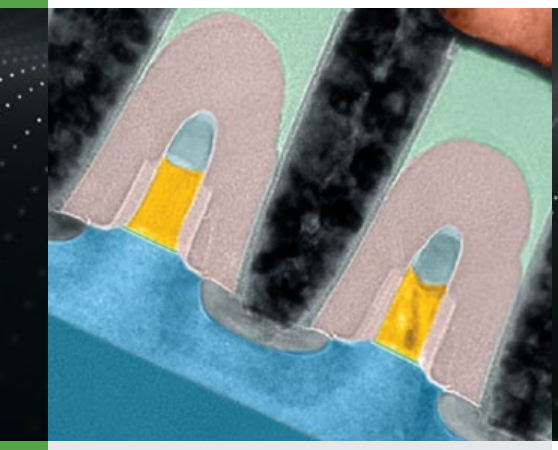

Cu-45HP

Advanced, SOI-based design system for high-performance applications

Highlights

- Take advantage of a proven design system
- Meet design goals by taking advantage of the intrinsic advantages of SOI technology
- Differentiate with dense eDRAM and high performance HSS for faster data access and transmission
- Access lead-edge design tools and methodology

A proven design platform

With Cu-45HP, you can leverage all the advantages of silicon-on-insulator (SOI) technology in a proven custom logic offering.

Our technology experts have led the industry in bringing SOI into volume manufacturing and have successfully delivered generations of high performance systems that exploit the technology. Cu-45HP capitalizes on this experience and a decade-plus of industry leadership in delivering ASICs for wired communications. Already successfully deployed by customers across a range of high-performance applications, the Cu-45HP design system offers a comprehensive platform for developing sophisticated semiconductor chips for mobile and wired networking equipment, cloud and data center hardware, aerospace and defense applications and other performance-driven solutions.

Performance, delivered

The Cu-45HP design system is based on our 45nm SOI technology. This technology offers performance advantages over bulk-based semiconductors because of the decreased junction capacitance provided by the oxide layer in SOI. Strained silicon techniques, such as embedded silicon germanium and dual strain liners, enhance the inherent SOI performance benefits.

Cu-45HP leverages dual logic oxide technology. The design system's 12-angstrom logic devices enable you to trade off performance and power; its 25-angstrom logic devices can help you effectively manage higher voltages for I/Os while still providing performance advantages over corresponding 65 nm devices.

Because SOI uses buried oxide isolation and floating bodies in lieu of well contacts, extremely high levels of integration are possible in Cu-45HP. Backed by our team's record of success in implementing large, complex semiconductors, you can confidently exploit this density advantage in developing advanced system-on-a-chip (SoC) solutions.

Differentiate your silicon

Cu-45HP offers an array of compilable eDRAM options that feature deep trench capacitors for superior soft error rate characteristics. Density-optimized eDRAM options are tuned for high bandwidth; performance-optimized options offer fast random-access cycle times.

Our cycle-time-tuned eDRAMs give you the flexibility of replacing small blocks of embedded SRAM (eSRAM) or low bit-count eSRAMs with eDRAM. Substituting eDRAM for eSRAM in your design can help you achieve lower leakage and integrate more on-chip memory in a smaller area—while preserving performance.

A broad spectrum of compilable eSRAMs is available. The SRAMs offer added design flexibility, providing you with the ability to make tradeoffs for active and standby current, area, bandwidth, latency and performance. The variety of possible memory configurations enables extensive customization for optimized SoC memory solutions.The Cu-45 intellectual property (IP) portfolio also includes:

- HSS cores, supporting a broad range of industry standards and offering superior jitter and equalization characteristics
- IBM PowerPC® embedded processors, optimized for scalability and performance in SoC designs. Additional IP building blocks and design enablement resources are available directly and through third party suppliers.

Designed to enable first-pass design success

Cu-45HP is designed to help you achieve first pass design success. Statistical timing techniques, holistic design approaches and the ability to leverage both industry-standard and innovative Avera Semi tools and models provide you with a myriad of options to overcome the challenges of designing in advanced technology nodes. Our end-to-end design strategy— featuring concurrent chip and package design, an integrated noise- and power-analysis environment and at-speed structural test—can help you verify design performance and design around potential pitfalls before they become issues in system-level hardware.

Features and specifications

Cu-45HP features:

- Dual logic oxide technology, with 12-angstrom logic devices for performance advantages and 25-angstrom logic devices for I/Os
- Multiple Vt and multiple track-height design libraries for density, power and performance tradeoffs and advantages
- Up to a 7x reduction in the soft error rate (due to the smaller size of the well area between the drain and source of SOI-based transistors compared with bulk CMOS devices)
- A broad selection of packaging options

Cu-45HP at a glance	
Process generation (nm)	45
Technology	SOI
Supply voltage VDD (V)	1.0/0.9
Wireable gates (millions)	Approximately 200
Total levels of metal	9 – 10
Thin-level dielectric	Ultra low-k
Multi-Vt design libraries	12 track: Regular 9 track and 12 track: High, super high and ultra high
eDRAM compilers	• Multi-banked, bandwidth optimized eDRAM • Pseudo two-port eDRAM • Fast random cycle eDRAM (SRAM alternative)
Other memory compilers	• High-performance compilable one-port SRAM • Ultra high-performance compilable one-port SRAM • Compilable dual-port SRAM • Compilable two-port SRAM • Register array (two port, four port) • Register file (one port, two port, ultra-high density two port) • Compilable ternary CAM • Compilable ROM
HSS cores	Broad range of offerings, supporting more than a dozen industry standards
Power-management options	Base: • Multi-Vt design libraries (trade off power and performance) • Multi track-height design libraries • Clock gating (by design or through synthesis) • Power supply flexibility (IP in voltage islands can use different supply voltages) • Selective voltage binning • Low-power SRAMs
	Semi-custom:* • Voltage island power gating (turn off unused areas of a chip)
	Full custom:† • Dynamic voltage scaling (modify power supply on-demand, with feedback) • Dynamic frequency scaling (modify clock on-demand, with feedback)

*Semi-custom: Base methodology provided as part of custom logic methodology, customization needed to support each product.

†Full custom: Developed on a product by product basis

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